MHz. Uncertainties associated with this measurement system are in the ac-dc difference of the TVC in the range of two ppm, lumped uncertainties due to the rest of the system also in the range of two ppm, and the standard deviation of the mean of fifteen observations in the range of one ppm.

To minimize dc uncertainties, the digital voltmeter used in the step calibration is calibrated by the dc source used as a reference for the thermal measurements. This source is thus considered the dc reference for both measurements.

The estimated standard deviations of the step and thermal calibrations were computed by

$$U = \left(a^2 + \frac{(\Sigma\, b_i^2)}{3} \right)^{\frac{1}{2}}$$

where

a=standard deviation of the observations, and

b=limits of the estimated errors.

The resulting standard deviations are 1.6 ppm for the step calibration and 1.9 ppm for the thermal measurement.

Results of step and thermal measurements of digitally synthesized source **12** are shown in FIGS. **4–7**. To demonstrate the performance of different units under various operating conditions, two sources DSS1 and DSS2, (not shown) were measured using both internal and external clocks (not shown) to synthesize one hundred twenty-eight step sine wave approximations (FIGS. **4, 5** and **6**). As a further demonstration, the results of measurements on a nonsinusoidal waveform (sine wave approximation with thirty percent third harmonic) are shown in FIG. **7**. The plots show the average difference between three sets of measurements consisting of two step calibrations (represented by the dashed line) and five thermal measurements (plotted points with one-standard deviation error bars) at each frequency.

Agreement between the two methods is better than five ppm from 30 Hz to about 2 kHz. Above 2 kHz the rms value of digitally synthesized source **12** is less predictable, becoming increasingly dependent on the bandwidth adjustment described above. It was, however, possible to trim the rms value of DSS2 between 30 Hz and 15 kHz to within ten ppm of the calculated value. This "flatness" adjustment appears to be very stable vs. time and has proven to be relatively immune to normal mechanical shocks encountered during shipment.

In testing the preferred embodiment of the present invention, the rms value of a digitally synthesized waveform may be estimated by measuring the dc level of each of the steps used to generate the waveform. The accuracy of this estimate depends on the difference between the static and dynamic performance of the digital to analog converters MDAC **20** and **22**. To minimize glitches caused by MDAC **20** and **22**, due to charge injection and switching skews, a deglitching circuit which uses a fast switch, switches **24, 26, 28** and **30**, to toggle between MDAC **20** and **22** is utilized. This circuit substantially improves the step quality while increasing the effective frequency range of the source.

The calculated rms value agrees with the thermally measured value to within five ppm from 30 Hz to 2 kHz. In this frequency range the digital-synthesis/calculation technique reenforces the validity of the traditional thermal approaches and may be considered as an independent dc-to-ac transfer standard. At higher frequencies, digitally synthesized sources are increasingly dependent on components, but it may be precisely adjusted so that the flatness of its rms value vs frequency is within ten ppm out to 15 kHz. With faster digital to analog converters used in place of MDAC **20** and **22**, it should be possible to extend this performance to higher frequencies.

While the present invention has been described by way of a preferred embodiment, it is to be understood that this is for illustration purposes only and the present invention should not be limited thereto, but only by the scope of the following claims.

What is claimed is:

1. A digitally synthesized source for synthesizing a sinusoidal voltage waveform comprising:

a read only memory storing digital values representing sine waveforms;

clock means for generating first and second pulse trains such that while said first pulse train is high, said second pulse train is low and while said second pulse train is high, the first pulse train is low;

first latch means connected to said clock means and said read only memory and responsive to said first pulse train to provide as output digital values stored in said read only memory;

a first converter means connected to said first latch means for receiving and converting digital values stored in said read only memory into a first output current step signal in response to pulses of said first pulse train;

second latch means connected to said clock means and said read only memory and responsive to said second pulse train to provide as output digital values stored in said read only memory;

a second converter means connected to said second latch means for receiving and converting digital values stored in said read only memory into a second output current step signal in response to pulses of the second pulse train;

an operational amplifier having an inverting input, a non-inverting input and an output;

switch means for alternatively connecting said first converter means and said second converter means to said inverting input and said non-inverting input under control of said first and second pulse trains such that one of said first and said second current step signals is connected to said inverting input while the other is connected to said non-inverting input; and

a feedback connection between said output and said inverting input of said operational amplifier through a variable capacitance, said variable capacitance being set to a low value for eliminating frequency components above 10–20 MHZ in the voltage waveform and for trimming a bandwidth of the operational amplifier so that a RMS value of the voltage waveform is flat within the audio-frequency range of the voltage waveform.

2. The digitally synthesized source according to claim **1** also including connector means for connecting said non-inverting input to ground.

3. The digitally synthesized source according to claim **1** wherein said switch means includes CMOS switches.

4. The digitally synthesized source according to claim **1** wherein said first and said second converter